RF W-Band Wafer-to-Wafer Transition

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***Abstract*—Multiwafer silicon designs must provide an avenue for electrical signals to flow from wafer to wafer. For this purpose, a two-layer electrical bond is proposed to provide electrical connection between two coplanar waveguides printed on the adjacent faces of two vertically stacked silicon wafers. In addition to serving as a versatile low-temperature thermocompression wafer bond, loss of approximately 0.1 dB is measured for this novel compact packaged wafer-to-wafer transition from 75 to 110 GHz.**

***Index Terms*—Micromachining, microwave circuits, packaging, wafer bonding.**

I. Introduction

WAFER bonding has been used commercially in applications such as power devices, silicon-on-insulator (SOI), sensors, die attachments, sealing, and other microelectromechanical system (MEMS) applications [1]–[4]. Its use has become prevalent due to the many technical and economic advantages afforded. For example, specialty wafers may be used for some devices while silicon may be used for the main circuitry, and fabrication compatibility issues may be circumvented by processing separate wafers. Commercially, these advantages translate to economic benefits as well since well-founded processing lines need not be disrupted.

There are three main classes of bonding: anodic, fusion, and intermediate. Anodic bonding involves glass to silicon bonding at temperatures up to 500 °C and potentials from 100 V to 1 kV. An application of this process is a sensor chip for a MEMS automotive accelerometer [3]. The second main class of bonding, i.e., fusion bonding, is also known as silicon-to-silicon direct wafer bonding (DWB) and requires either hydrophobic or hydrophilic silicon surfaces be brought into contact and annealed at temperatures up to 1000 °C. In the hydrophobic case, a van der Waals force creates the initial pre-bond, while in the hydrophilic case, hydrogen oxide (OH) facilitates the pre-bond. Although the high temperatures required for this bond make it incompatible with microelectronic circuits, it is currently used for multiwafer microstructures like accelerometers and micromachined turbines [5]. Lastly, intermediate bonding involves mating wafers with an intermediate film be it glass, polymer based, or metal. Glass–frit bonding temperatures are generally 400–500 °C and, like all spin-on processes, thickness control is an issue. Alternatively, in intermediate metal-based bonding, various metals have been applied such as Ti, $TiSi_2$, PtSi, and $CoSi_2$ [1] with reported bond temperatures up to 700 °C. High-temperature wafer-to-wafer bonding may be deleterious to complex circuits by allowing dopant diffusion, reducing conductivity, and/or modifying physical circuit dimensions. Thus, there is a need to develop a low-temperature wafer-to-wafer bond that allows mating of micromechanical structures and other complex circuits without compromising electrical performance.

Low-temperature wafer bonding has been under study mainly for die attachment and electrical interconnects with the bulk of research centered on the eutectic or lowest melting temperature [2], [1], [4]. Of the eutectic-solder-based bonding, eutectic gold wafer bonding at 363 °C has been most highly promoted due the low minimum liquidus temperature and widespread use in die bonding. However, these bonding studies, e.g., by Wolfenbuttel and Tiensuu [2], [1], [4], focus on the bond itself and ascertain bond quality through visual inspection of grain boundaries or load measurements. Electrical measurements including the bond are not performed, thus circuit performance is not a consideration in these studies.

Classical electrical interconnects for monolithic-microwave integrated-circuit (MMIC) packages or integrated-circuit (IC) chips are wire bonds. Although most commercial IC chips are wire bonded today, the bonds have large parasitic effects, which are difficult to compensate for. To overcome this problem, solder bumped flip-chip technology has produced greater packaging density and improved performance, due to shorter leads, lower inductance, and improved noise control. The solder used is typically 80% Au–Sn, 60% Sn–Pb, or 100% In, and requires reflow of solder for self-alignment at temperatures close to 280 °C. Additionally, the solder bump height is on the order of 20–40 μm.

As compared to wire-bonding and flip-chip technology, the thermocompression bond, at temperatures below the eutectic, compares quite favorably. The 1–4-μm electroplated bumps are comprised of the same material as the circuit metal and, thus, produce little mismatch in thermal expansion at the bond temperature. The bumps do not flow during compression as would solder and, additionally, thermocompression bonds for packaging applications would yield little out-gassing for low-temperature vacuum bonding as compared to solder or glass alternatives [6]. Finally, thermocompression bonds of the type presented here have been tested in lap shear at Massachusetts Institute of Technology (MIT), Cambridge, with bond strengths comparable to that of wire bonds [6]. Unlike many previous wafer-to-wafer silicon–gold-bond investigations, the goal of this paper is not only to develop a low-temperature

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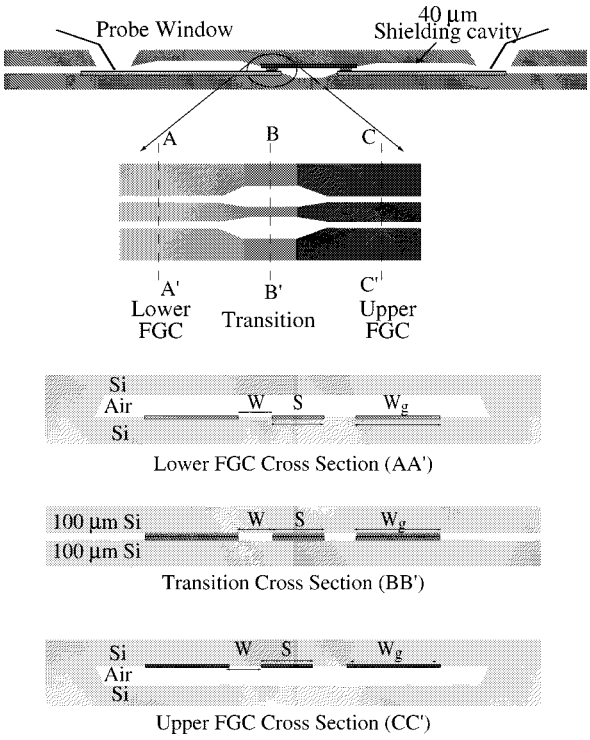


Fig. 1. Illustration of wafer-to-wafer transition.

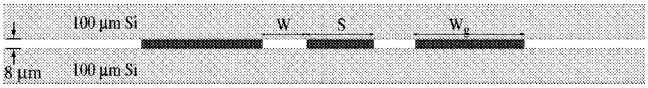


Fig. 2. Schematic for Maxwell 2-D RF interconnect simulation.

TABLE I
CHARACTERISTICS OF FEED LINE AND TRANSITION GEOMETRIES

	Feed Line (AA',CC') (40-24-106 μm)	Trans 1 (BB') (20-44-100 μm)
Gold (μm)	1	8
Upper Si	no	yes
C_{sub} (F)	1.7×10^{-10}	2.14×10^{-10}
C_{air} (F)	2.7×10^{-11}	2.22×10^{-11}
ϵ_{eff}	6.3	9.6
Z_o (Ω)	49.9	48.4
	Trans 2 (BB') (30-59-100 μm)	Trans 3 (BB') (40-65-100 μm)
Gold (μm)	8	8
Upper Si	yes	yes
C_{sub} (F)	2.1×10^{-10}	2.15×10^{-10}
C_{air} (F)	2.12×10^{-11}	2.15×10^{-11}
ϵ_{eff}	9.9	9.9
Z_o (Ω)	50	48.8

gold-to-gold wafer bond, but to develop an RF electrical connection from one silicon wafer to another at W-band.

II. DESIGN

Fig. 1 illustrates the transition concept and measurement method as a back-to-back configuration. In this measurement scheme, a single finite ground coplanar (FGC) line transitions from lower to upper wafer, and then back to the lower wafer for on-wafer probing. Probe windows are micromachined through the upper 100-μm wafer, and 40-μm air cavities are micromachined around the FGC line for protection. The lower (AA') and upper (CC') FGC cross sections have dimensions of 40-24-106 μm (S–W–W$_g$) and line thickness of 1 μm while the transition region (BB') includes an additional 3 μm of gold on both sides to ensure wafer-to-wafer contact. Once in contact, the gold of BB' is 8-μm tall and sandwiched between the silicon wafers, thereby changing the shunt capacitance, effective dielectric constant, and characteristic impedance of the line at the transition region. To design a transition with good RF performance at W-band, the transition geometry must be modified to preserve the original 50-Ω characteristic impedance.

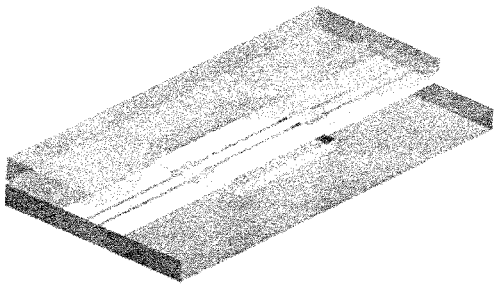
Electrostatic simulations show that a 50-Ω line may be achieved in the transition region (BB') by making minor changes to the FGC feed-line dimensions.[1] Fig. 2 illustrates the modeled two-dimensional cross section. The capacitance is computed twice for the FGC mode of interest: once as shown in Fig. 2, producing $C_{\rm sub}$, and once with all substrates replaced with air $(C_{\rm air})$. For the FGC mode, the center conductor is considered at 1-V potential, and the ground planes at zero potential. The effective dielectric constant and characteristic impedance are calculated using static equations. As shown in Table I, line characteristics for the feed and three 50-Ω transition geometries of Fig. 1 are shown. Note, all transition geometries yield $\epsilon_{\rm eff}$ from 9 to 10, while that of the feed line is 6.3.

The total circuit length for all full-wave finite-element method (FEM) simulations is 1820 μm with two 100-μm-long transition sections. The 30-59-100-μm transition geometry is analyzed considering finite conductivity of 4.1×10^7 S/m, and results in insertion and return losses of 0.85 and -20 dB, respectively. The geometry is shown in Fig. 3(a), with a curved cut-out of the upper silicon wafer for view of the transition. The simulated S-parameters of the 30-59-100-μm transition are shown in Fig. 3 in addition to the S-parameters of a through line of the same length. The difference in insertion loss between the back-to-back transition and through line is 0.166 dB, implying 0.083-dB insertion loss per transition. Simulations for the back-to-back 40-65-100- and 20-44-100-μm transitions yield similar results of 0.82- and 0.77-dB insertion loss with -20.13- and -22.55-dB return loss at 94 GHz, respectively, as shown in Fig. 4. As compared to the through line, the loss of the 40-65-100-μm transition is 0.068 dB, and the loss of the 20-44-100-μm transition is 0.043 dB. Table II summarizes these results, showing estimated loss of each of the three transitions to be $<$0.1 dB.

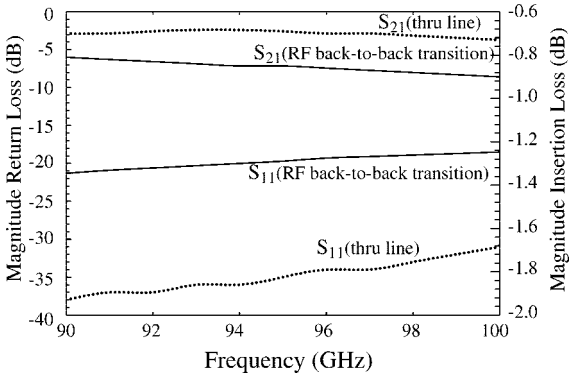
III. FABRICATION

Fabrication involves two-sided processing, probing windows, finite ground coplanar air cavities, and alignment marks. The fabrication process flow includes fabrication of the upper and lower 100-μm high-resistivity (3000 $\Omega\cdot$ cm) silicon wafers with thermally grown SiO_2 on both sides.

[1]Maxwell 2-D, Ansoft Version 1.9.04, Pittsburgh, PA, 1997.



(a)



(b)

Fig. 3. HFSS simulation results for RF back-to-back interconnect with 30-59-100-μm transition, as compared with through line of same length. Finite conductivity of 4.1 $\times$ 10^7 S/m is used. (a) Schematic. (b) Simulated S-parameters.

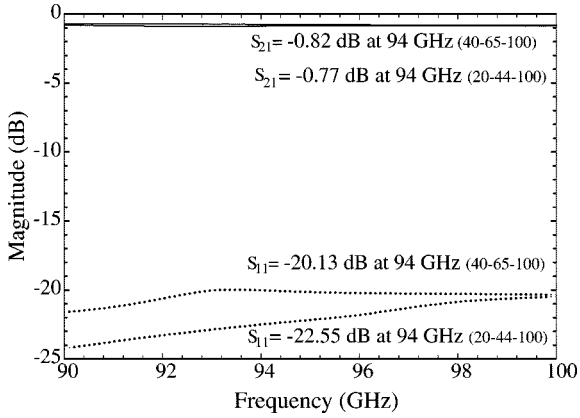


Fig. 4. HFSS simulation results for RF back-to-back interconnect with 20-44-100- and 40-65-100-μm transition. Finite conductivity of 4.1 $\times$ 10^7 S/m is used.

As shown in the right column of Fig. 5, the lower wafer fabrication begins with metallization of the frontside alignment marks and circuit metal using liftoff of chrome/gold (Cr/Au) (500/9500 Å). Oxide is then patterned for cavities using buffered hydrofluoric acid (BHF) at an etch rate of 1000 Å/min. Electroplating of the RF interconnects commences with patterning a thin photoresist layer, after which a seed layer of Cr/Au/Cr (500/1000/500 Å) is flood evaporated, patterned, and electroplated in a cyanide-based solution to approximately 3 μm. Removal of the seed layers completes the RF interconnect formation, and the final step is to anisotropically etch the oxide-patterned cavities in potassium hydroxide (KOH) to a depth of 40 μm.

TABLE II
BACK-TO-BACK RF WAFER-TO-WAFER TRANSITION SUMMARY OF THEORETICAL SIMULATIONS

Simulation	Fig.	S_{21} (dB)	S_{11} (dB)	Trans. Loss (dB)
Through	3(b)	0.684	36	n/a
20-44-100	4	0.77	23	0.043
30-59-100	3(b)	0.85	20	0.083
40-65-100	4	0.82	204	0.068

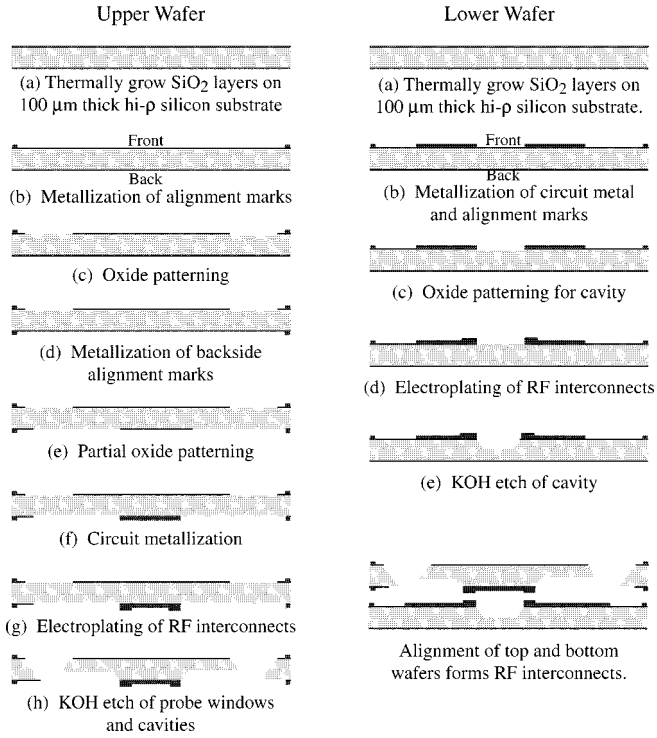


Fig. 5. Fabrication of upper and lower 100-μm silicon wafers for RF interconnects.

The upper wafer is fabricated in a similar manner and allows for probe windows needed for measurements, as illustrated in the left-hand-side column of Fig. 5. After metallization of frontside alignment marks using liftoff of Cr/Au (500/2000 Å), oxide is patterned for the probing windows. These two processes are repeated on the backside of the wafer using infrared (IR) alignment, with protective cavities patterned in addition to probing windows. Electroplating of the RF interconnects is completed using the same method described for the lower wafer, while the oxide-patterned cavities and probe windows are anisotropically etched in KOH. In this case, the probe windows must be etched through the 100-μm wafer and the cavities need only be etched 40 μm. For this reason, the choice of KOH becomes useful as it etches oxide at a rate of 14 Å/min or 840 Å/h, allowing a thin film of oxide to protect the cavity regions from the etchant until 60 μm is etched in the probe window regions. In this way, two different etch depths may be obtained during one etch.

There are two wafer fabrication processes that may affect alignment and bonding of the upper and lower wafers: elec-

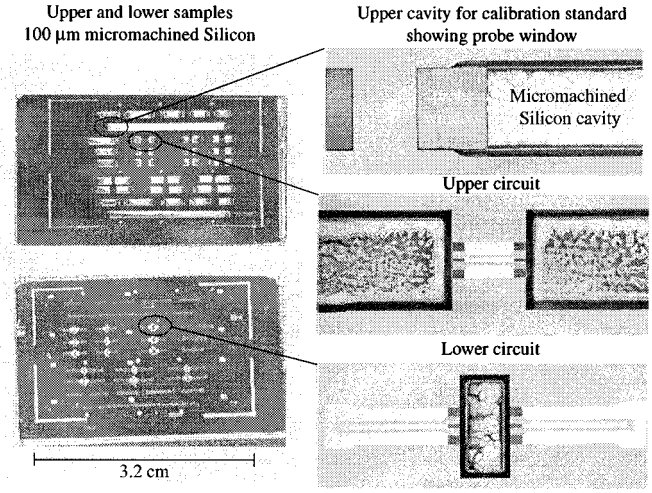


Fig. 6. Photographs of fabricated circuits.

troplating and alignment. The issue with electroplating is the ability to uniformly control the electroplated bump height. Electroplating solution, current, wafer placement, and cleanliness are all contributing factors. As observed experimentally, the estimated roughness of the electroplated gold is ± 0.3 μm. Wafer alignment from one side to the other is achieved using conventional IR alignment techniques, in which typical IR alignment error is ± 5 μm. Special attention is given to both the electroplating and IR alignment steps to ensure wafer-to-wafer contact and alignment.

Photographs of fabricated circuits are seen in Fig. 6. The left-hand-side column shows the upper and lower 100-μm silicon samples of dimensions 1.9 cm $\times$ 3.2 cm, and the right-hand-side column of Fig. 6 displays an upper micromachined air cavity for a calibration through line. The probing window, which allows probing through the 100-μm upper wafer to the circuit on the lower wafer, is also shown. A close-up of one RF wafer-to-wafer transition is shown as a combination of the upper and lower wafers.

IV. Wafer Alignment and Thermocompression Bonding

A. Bonding Considerations

There are essentially three silicon wafer-to-wafer bonding techniques, as mentioned in Section I: anodic, direct, and intermediate-layer bonds. The latter technique includes bonding with polymer glue, soft glass, or metal. The bonding process for all techniques may be summarized as the following three-step sequence: surface preparation, contact, and annealing. The first step is important since the quality of the bond has a strong dependence on surface conditions. Intimate contact is made, after proper alignment, using pressure, which is followed by increased temperature. The type of bonding examined here may be categorized as intermediate-layer bonding, with the intermediate layer being gold, and, as reported in the literature [7], [4], [1], [2], [8], [9], has been referred to as thermocompression bonding, solid-state welding, diffusion welding, and eutectic brazing. The formation of a solid-state bond between joining metals is the common denominator. Hereafter, the bonding discussed and presented will be referred to as thermocompression bonding.

In thermocompression bonding, time, temperature, and pressure coalesce the base metals at temperatures below their melting point or melting range. While in intimate contact at the bonding temperature, atoms in the metal acquire increased energy, and after a specified period of time, the transport of atoms across the original interface results in a solid-state bond. As thermocompression bonding involves a range of temperatures, pressures, and deformations, it is difficult to present one comprehensive theory of the process. However, it is worthwhile to list and consider factors that may contribute to this process in an effort to understand the reasoning for the temperature, time, and pressure for the wafer-to-wafer transition of interest.

1) Forces of Attraction: To obtain adhesion, the two gold surfaces must be close enough to become mutually attractive. To take advantage of these attractive forces, the metals must be placed in intimate contact, e.g., using pressure. However, pressure alone, causing both plastic and elastic deformations, is not sufficient for bonding at room temperature. One reason for this may be surface contaminants, to be discussed in a following section. In addition to pressure, a means of bringing the atoms in close enough contact is through diffusion. As temperature is increased and the metallic atoms vibrate more energetically, a small fraction of them will relocate in the lattice, forming permanent bonds.

2) Pressure: Increasing pressure increases the amount of contact between the gold atoms, but increases risk of silicon substrate fracture and equipment damage. The silicon wafers used in this effort have been thinned from 500 to 100 μm, resulting in a more fragile sample. Also, applying pressure to a plate, as on a bonding machine, that is not perfectly flat due to circuit imperfections may cause that plate to stress fracture.

3) Temperature: Role of Diffusion: Increasing temperature enhances the diffusion mechanisms in the gold atoms. However, it is important to consider other materials present, and how they will be affected by increases in temperature. In this case, the main concern is silicon, and its eutectic point with gold. The silicon–gold alloy is formed by solid-liquid interdiffusion at the interface, followed by solidification upon cooling. This point is located at 363 °C for gold–silicon and corresponds to a eutectic composition of 2.85% Si and 97.1% Au by weight. Eutectic bonding is currently used for die bonding and multiwafer assembly [4], [1], [2], as an alternative to high-temperature bonding. However, to maintain purity and highest conductivity of the gold electrical contacts, which are part of the circuits themselves, it is highly undesirable to allow silicon diffusion into the gold or vice versa. Additionally, it is important to maintain the dimensions of the gold lines, as they define the characteristic impedance. For this reason, the bonding temperature for the gold-to-gold diffusion is kept to 350 °C, 13 °C below the silicon–gold eutectic.

4) Effect of Surface Contaminants: Since deformation welding generally produces sufficient intimate contact for a metallic bond, it may be concluded that surface films and contaminants are responsible for failed bonding attempts [10], [11]. There are two general groups of surface films: oxide films

and adsorbed organic and water vapor films. Oxide films are relatively brittle and hard compared to metals while adsorbed films tend to be more elastic. Both films may be present on a metallic surface.

Most metals, with the exception of gold, react with atmospheric oxygen to form native oxide layers 20–100 Å. Essentially only a few seconds of atmospheric contact is sufficient to produce this oxide layer. This has been found experimentally [10], [11] and suggests that adsorbed organic films may be the cause of bonding difficulty with regard to gold thermocompression bonding. Jellison [10], [11] examined the effect of surface contamination on thermocompression bonding of gold. On two groups of gold samples, Auger electron spectroscopy indicated carbon as the primary surface impurity. Nitrogen traces were found on one group suggestive of residual photoresist. Exposure to ultraviolet radiation has shown a significant reduction of these surface contaminants and improved bond strength. Additionally, ultraviolet cleaning before bonding reduces the temperature required for thermocompression gold-bond formation.

B. Experimental Setup

Since high-pressure and uniform heating are required for the bonding process, commercial wafer bonding equipment is used for this effort.[2] The experimental alignment and bonding procedure begins as follows. To prevent surface contamination, the wafers are cleaned with organic solvents and then ultraviolet (UV) exposed for 30 min. Aligned silicon wafer bonding is a two-step process utilizing two pieces of commercial equipment. First, the wafers are aligned in the EV420 Manual Aligner. Once aligned, the wafers are brought into close proximity and clamped together in the bond fixture, which is then loaded into the vacuum bond chamber of the EV 501 Manual Wafer Bonder. Once in the bond chamber, the following sequence of events occurs. First, a nitrogen ambient of 10^{-2} bar is achieved in order to maintain a low particulate environment and prevent any oxidation. A small amount of pressure, i.e., 50 N, is then applied to the samples, while the top and bottom bond plates heat up to 350 °C. Once temperature has stabilized, 200 N are applied for 30 min.

V. Measurements

S-parameters of the RF wafer-to-wafer transitions are measured on an HP 8510C Network Analyzer[3] using 150-μm pitch Picoprobes.[4] A thru-reflect line (TRL) calibration method is utilized to deembed the probe-to-wafer transition and establish reference planes at the input and output ports of the circuits under test [12], [13]. The interconnects are tested in a back-to-back configuration, with a short section of transmission line connecting them. Fig. 7 shows a photograph of the RF back-to-back circuit with Transition 2 (30-59-100 μm) revealing placement of the reference planes just at the onset of the transition, 800 μm in from each probe. The S-parameter measurements for each RF wafer-to-wafer transition will, therefore, show the insertion loss of two 100-μm transitions and a 400-μm midsection of feed line.

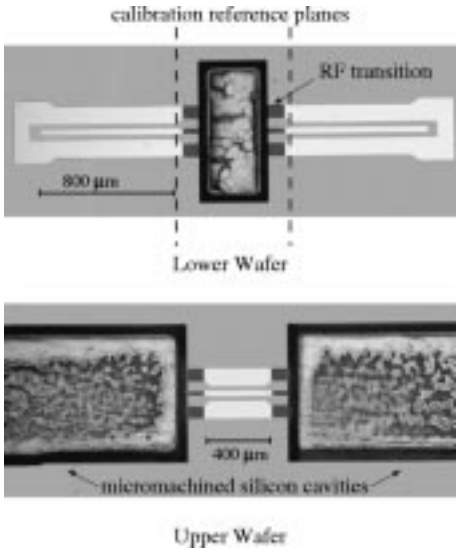


Fig. 7. Photograph of RF wafer-to-wafer transition showing placement of calibration reference planes.

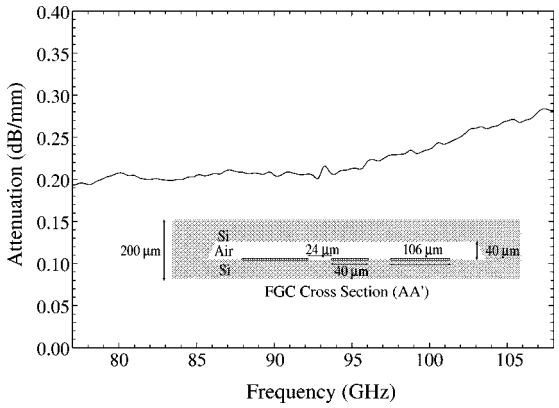


Fig. 8. Measured attenuation for FGC line.

At 94 GHz, the attenuation of the 50-Ω feed line, with cross-section AA' is 0.22±0.02 dB/mm, as shown in Fig. 8. Note the measured line is packaged with a 40-μm air cavity, as shown in the imbedded cross section. Thus, the expected loss from the 400-μm midsection of feed line is approximately 0.09±0.01 dB.

Fig. 9 reveals back-to-back transition measurements for the three transition geometries, with return loss plotted on the left-hand-side axis and insertion loss plotted on the right-hand side. From 90 to 98 GHz, the insertion loss for transition 1 ranges from 0.32±0.02 dB with return loss below −30 dB. Subtracting the line loss of 0.09 dB from the total insertion loss yields 0.23±0.03 dB loss for the two transitions. Thus, the loss per transition may be approximated as 0.13±0.02 dB per transition. Table III summarizes the results from 90 to 98 GHz with transition loss ranging from 0.07 to 0.15 dB with an error of ±0.02 dB. This minimal 0.02-dB loss variation is due to errors introduced by probe contact repeatability and calibration errors. Transition 3 yields the best results due to the fact that geometry modifications were made only to the aperture widths

[2]Electronics Visions, Phoenix, AZ. [Online]. Available: http://www.elvisions.com

[3]Hewlett-Packard Company, Santa Clara, CA.

[4]GGB Industries, Naples, FL.

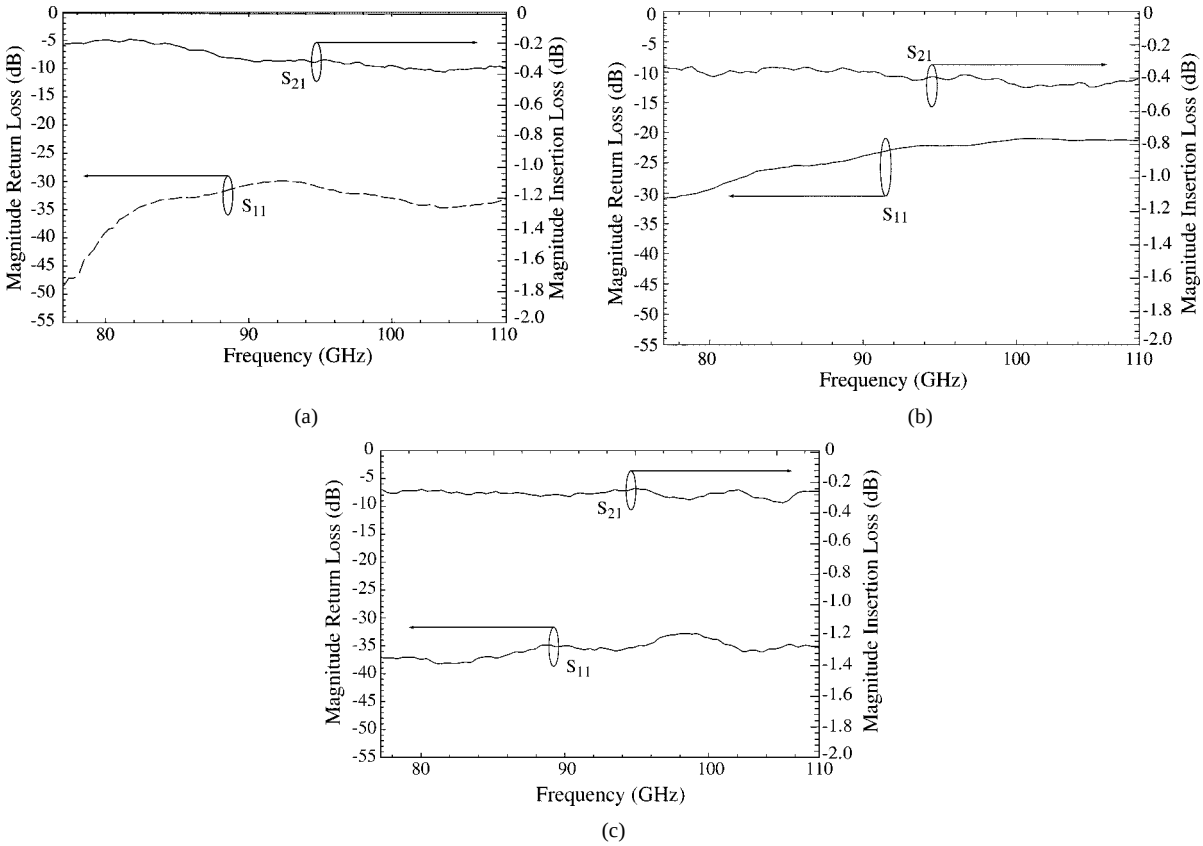


Fig. 9. S-parameters of measured RF wafer-to-wafer transitions. (a) 20–44–100 μm. (b) 30–59–100 μm. (c) 40–65–100 μm.

TABLE III
BACK-TO-BACK WAFER-TO-WAFER INTERCONNECT MEASUREMENT SUMMARY FROM 90 TO 98 GHz

Geometry	Fig.	S_{21} (dB)	S_{11} (dB)	Trans. Loss (dB)
20-44-100	9(a)	0.32 ± 0.02	≤ 30	0.13 ± 0.02
30-59-100	9(b)	0.38 ± 0.04	≤ 20	0.15 ± 0.02
40-65-100	9(c)	0.24 ± 0.04	≤ 30	0.07 ± 0.02

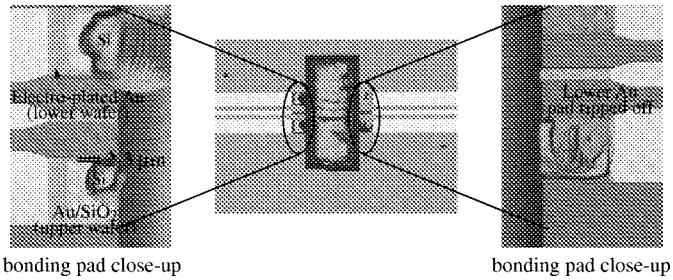


Fig. 10. Photograph of bonded sample after wafers pulled apart showing bonding and alignment.

while maintaining the 40-μm center conductor width of the feed line, thereby reducing the added transition parasitics with the continuity of the center conductor width.

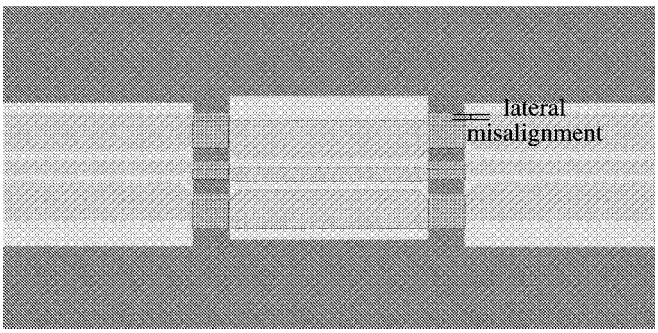


Fig. 11. Schematic of simulated lateral misalignment.

VI. BOND EVALUATION AND ANALYSIS

A simple bond and alignment evaluation is obtained using IR inspection, in which the bonded pads are observed through the silicon layers. Fig. 10 shows photographs of the bonded circuit of transition 1 after being pulled apart. The gold bond is strong enough to rip the upper gold pads off the upper silicon wafer, taking silicon dioxide and some silicon with it. Misalignment on the order of 2–3 μm is shown.

A. Misalignment

To determine the importance of lateral alignment, a parametric study is performed for two of the three wafer-to-wafer transitions. For each geometry, HFSS simulations are run in which the top wafer is laterally shifted with respect to the

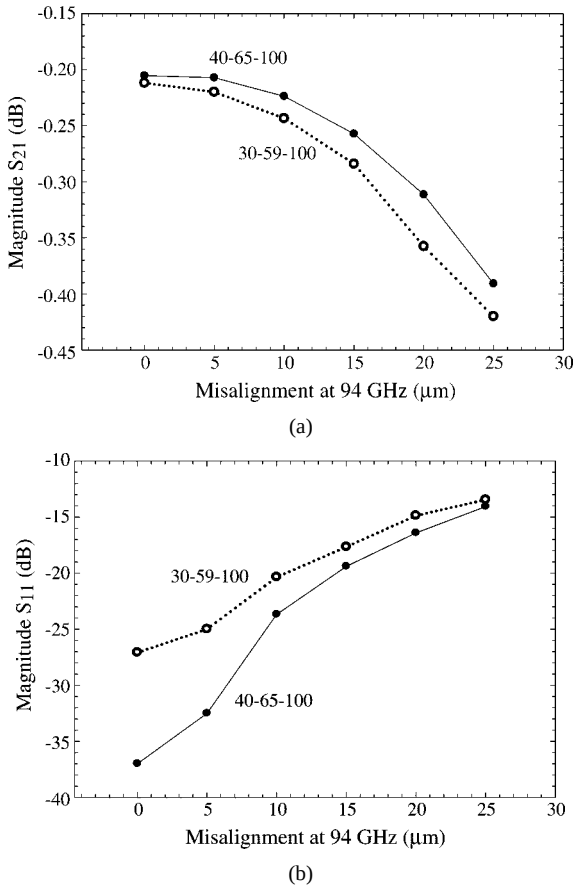


Fig. 12. Simulated scattering parameters as a function of misalignment at 94 GHz for Transitions 2 and 3. (a) Insertion loss. (b) Return loss.

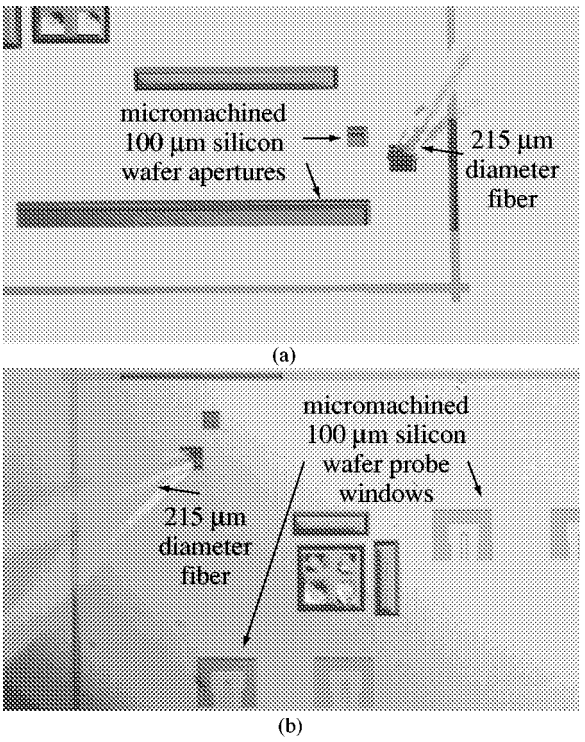


Fig. 13. Photos of 215-μm-diameter optic fibers threaded through two Si wafers.

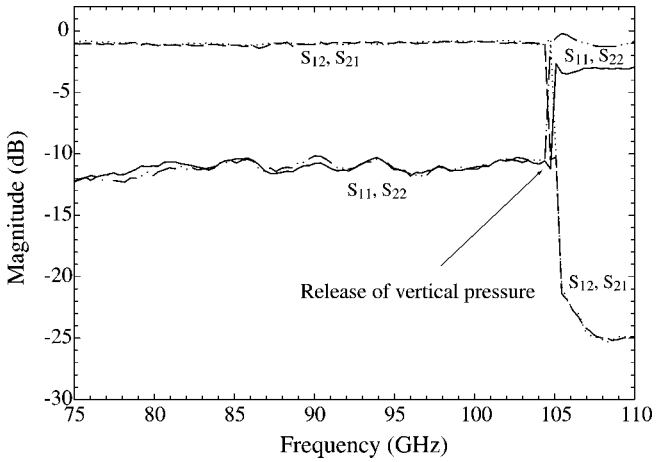


Fig. 14. S-parameter measurements of unbonded RF wafer-to-wafer transition.

lower wafer by increments of 5 μm until the center conductors no longer touch. A lateral misalignment schematic is shown in Fig. 11. Examining Fig. 12(a), insertion loss for the 40-65-100-μm transition varies from 0.2 dB (aligned) to 0.22 dB at 25% misalignment, and 0.5 dB with 75% misalignment. As misalignment varies from 0% to 100% from the center conductor, insertion loss varies by 0.35 dB for this transition. Examining the corresponding return loss values, shown in Fig. 12(b), 25% misalignment (10 μm) yields $-$24-dB return loss, while a 75% misalignment yields $-$13-dB return loss. With return and insertion losses ranging from $-$13 to 40 dB and from 0.2 to 0.55 dB, respectively, it may be concluded that lateral misalignment is not critical to circuit performance, but modifies insertion loss by up to 0.35 dB. A similar result is found from the 30-59-100-μm transition, with insertion loss values ranging from 0.21 to 0.5 dB.

B. Contact

Early in this study, wafer-to-wafer alignment was attempted by anisotropically etching holes through the wafers and then threading them together with flexible fiber-optic cable. The fibers are uniformly 215-μm diameter, making the undercut of the anisotropic etchant a critical factor. A photo of the fibers threaded through two silicon wafers is shown in Fig. 13. After being threaded and, therefore, aligned, silver epoxy was placed along the sides of the two samples, and they were then put in an oven at 110 °C with a relatively light weight on top of them for pressure and curing.

Measurements of these circuits were unfavorable due to insufficiently low pressure and temperature, although the application of temporary pressure during measurement provided considerable improvement. Fig. 14 shows the measurement with the application of pressure from 75 to 105 GHz, and the deleterious effect of releasing that pressure from 105 to 110 GHz. This measurement illustrates the importance of strong gold-to-gold wafer bonds, as the application of pressure yields 1-dB insertion loss, yet without it, there is insufficient RF coupling for signal flow.

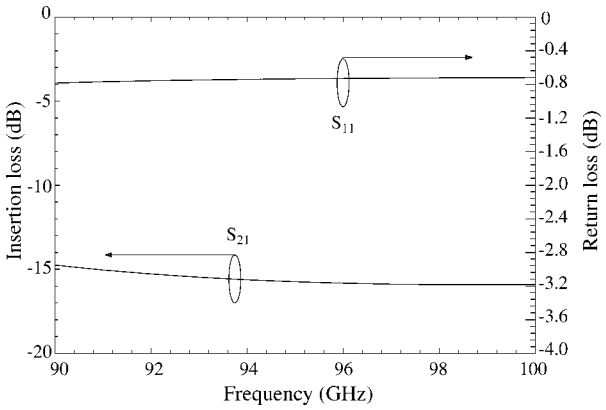


Fig. 15. S-parameter simulations of RF wafer-to-wafer transition with 2-μm vertical separation.

TABLE IV
WAFER-TO-WAFER INTERCONNECT LOSS SUMMARY FROM 90 TO 98 GHz

Geometry	Meas (dB)	Fig.	Sim (dB)	Fig.
20-44-100	0.13	9(a)	0.04	4
30-59-100	0.15	9(b)	0.08	3(b)
40-65-100	0.07	9(c)	0.07	4

Simulation of the wafer-to- wafer transition with 2-μm vertical separation verifies this result, as shown in Fig. 15. From 90 to 100 GHz, the circuit is essentially open with insertion loss of 15 dB.

VII. SUMMARY AND CONCLUSIONS

Table IV summarizes the measured and simulated results for each of the three transition geometries under consideration. All three geometries yield similar measured results ranging from 0.07- to 0.15-dB loss per transition. The 0.08-dB variation is due to the variation in the geometries themselves, the alignment, and the bond quality, with measurement error contributing no more than 0.02 dB.

Thus, alignment and bonding are the most important criteria to obtaining repeatable results. Simulations indicate that direct contact is critical. Misalignment, of the width of the center conductor affects insertion loss by 0.1 to 0.3 dB at W-band. Both measured and simulated results show the need for high-pressure low-temperature bonding, and without it, RF coupling is insufficient for signal flow.

In conclusion, on-wafer S-parameter measurements of a W-band RF wafer-to-wafer interconnect are demonstrated with average loss per transition of 0.12 dB. The thermocompression bond used for the interconnect is not only a strong low-temperature gold-to-gold wafer bond, but an excellent RF electrical connection. In addition, the approach is compatible with MMIC technology and may assist in the utilization of high-density multilevel integration schemes.

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